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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/670,634	09/25/2003	William J. Taylor JR.	SC12856TP	6860
23125	7590	05/10/2004	EXAMINER	
FREESCALE SEMICONDUCTOR, INC. LAW DEPARTMENT 7700 WEST PARMER LANE MD:TX32/PL02 AUSTIN, TX 78729			BREWSTER, WILLIAM M	
			ART UNIT	PAPER NUMBER
			2823	

DATE MAILED: 05/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 10/670,634	<b>Applicant(s)</b> TAYLOR ET AL.	
	<b>Examiner</b> William M. Brewster	<b>Art Unit</b> 2823	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
  - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
  - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
  - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 14 April 2004.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-22 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                        | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)               | Paper No(s)/Mail Date. _____  |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>092503</u> .  | 6) <input type="checkbox"/> Other: _____                                    |

**DETAILED ACTION**

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4, 8, 9, 11-16, 20-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Wu, U.S. Patent No. 5,856,226.

Wu anticipates a method of forming a semiconductor structure comprising: in fig. 1A, providing a substrate 1; introducing a dielectric region 2 within the substrate to laterally electrically isolate the semiconductor structure;

limitations from claims 2, 15, 20: further comprising implementing said insulating layer as an oxide layer, col. 6, lines 9-36;

limitations from claim 11: further comprising: surrounding the semiconductor structure with a dielectric isolation region 2;

forming a control electrode 4 overlying said substrate, said control electrode including a sidewall, vertical edges of electrode; forming an insulating layer 3 that is adjacent to said control electrode and overlying said substrate; forming a sidewall spacer 5A, 5B, around said sidewall of said control electrode and in contact with said insulating layer;

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limitations from claim 3: further comprising implementing the sidewall spacer from at least one of silicon, silicon germanium, or germanium: silicon, col. 6, lines 9-36;

forming a current electrode diffusion region 7A, 7B, in said substrate substantially aligned to said sidewall spacer, col. 6, lines 10-36; in fig. 1C, exposing the semiconductor structure to a gaseous fluorine ambient to substantially remove said sidewall spacer and to add fluorine to said dielectric region, col. 6, line 50 - col. 7 line 2;

limitations from claims 4, 7, 14, 19: further comprising implementing said gaseous fluorine ambient with molecular fluorine, further comprising implementing said plasma from at least one of nitrogen trifluoride, xenon difluoride or molecular fluorine:  $\text{NF}_3$ , col. 6, line 50 - col. 7 line 2;

limitations from claims 8, 9: in fig. 1C, exposing the semiconductor structure to said gaseous fluorine ambient to substantially remove said sidewall spacer without substantially modifying said insulating layer, layer 3, underneath the control electrode 4 remains unperturbed, further comprising: etching said sidewall spacer with said gaseous fluorine ambient selective to said insulating layer, col. 6, line 50 - col. 7 line 2;

limitations from claims 12, 13: exposing the semiconductor structure to said gaseous fluorine ambient to substantially remove said sidewall spacer and to introduce fluorine into said dielectric isolation region; exposing said dielectric isolation region to a gas to improve insulating characteristics of said dielectric isolation region, inherently the entire structure is exposed to the plasma of the

dry etching, and some fluorine will diffuse into the dielectric region 2, col. 6, line 50 - col. 7 line 2;  
and forming an extension region 6A, 6B, to said current electrode diffusion region in said substrate, said extension region substantially aligned to said control electrode;  
limitations of claims 21, 22: providing at least two semiconductor structures; laterally isolating said at least two semiconductor structures with a dielectric region, wherein a first semiconductor structure and a second semiconductor structure of said at least two semiconductor structures are laterally adjacent: while Hori describes the method for making one transistor, many transistors with laterally isolating dielectric regions will have to be made for an LSI circuit, col. 1, lines 16-27.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 5-7, 10, 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hori.

Hori teaches in col. 6, line 50 - col. 7 line 2 a dry etch with a fluorine etching gas of  $\text{CH}_2\text{F}_2$  or  $\text{NF}_3$ . Hori does not elaborate on the chemistry or plasma physics of the dry etching as applicants are not required to explain all well known phenomenon. Proffered

as evidence, Wolf, V. I, pp. 546-51, does explain the chemistry and plasma physics. Wolf, on p. 548, fig. 7, and on p. 549, second and third paragraphs, dry etching further comprising implementing said gaseous fluorine ambient with atomic fluorine, and further comprising generating said atomic fluorine from a plasma: dissociating for example  $\text{CF}_4$  into  $\text{CF}_2 + \text{F}$  and then dissociating into  $\text{CO} + \text{F}_3$ . A similar dissociation occurs in a plasma with other molecular fluorine atoms.

For claim 10, Hori does not specify the selectivity of the dry etching, but as only the spacers are substantially etched, it would have to be high. The practitioner must optimize these values.

"Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art . . . such ranges are termed 'critical ranges' and the applicant has the burden of proving such criticality . . . More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation."

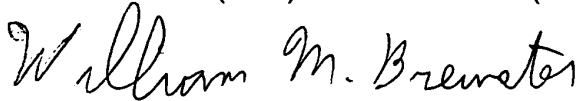
In re Aller 105 USPQ 233, 255 (CCPA 1955). See also In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmischer 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising there from. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William M. Brewster whose telephone number is 571-272-1854. The examiner can normally be reached on Full Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



6 May 2004  
WB